Solid State Electronics Center
Honeywell Inc.
12001 Highway 55
Plymouth MN 55441
612 954-2300

In reply refer to: 97CF-1022-0.35µm

22 October 1997

Naval Research Laboratory
4555 Overlook Avenue SW
Washington, D.C. 20375-5326

Attention: Harold Hughes, Code 6816

Subject: **CDRL A002 - Technical Progress Report - September 1997**
0.35 µm SOI CMOS Development

Reference: Contract Number N00014-97-C-2037

Dear Mr. Hughes:

In accordance with the terms and conditions of the referenced contract, Honeywell Inc., Solid State Electronics Center is pleased to submit the attached subject data item for the month of September, 1997.

Please feel free to contact Mr. Tim Whisler, Contract Representative, at (612) 954-2120, or Mr. Mike Liu, Program Manager, at (612) 954-2422, if you have any comments or technical questions.

Sincerely,

HONEYWELL INC.
Solid State Electronics Center

Connie Frey

Connie Frey
Program and Project Management

Attach.

cc: NRL 6800B
NRL 6810
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RADIATION HARD 0.35 μm SOI CMOS DEVELOPMENT (N00014-97-C-2037)

Report by M. Liu, PI (612)954-2422.
The work reported here was performed by D. Nelson, P. Green, J. Pifher, T. Fabien, J. Rekstad, and M. Liu.

PROGRESS FOR THE MONTH OF *September 1997*

We have started two quick turn DOI lots this month with objectives of completing unit processing required for gate oxide reduction and drain engineering. One five-wafer NMOS DOI lot and one five-wafer PMOS DOI lot were being processed at the same time using 22009883 design for quick turn evaluation of 0.8 μm devices with minimum geometry down to 0.5 μm (Note: SSEC has requested a new DOI design in mid-October specifically designed for 0.35 μm CMOS). New masks for 0.35 μm devices evaluation will be available in November. Electrical assessment of the parameters relevant to 0.35 μm CMOS will be evaluated accurately afterward.

We have pulled two wafers out of each lot (NMOS 9883-466 and PMOS 9883-467) at the silicide step for electrical testing to check for well dopings against process simulation. All other wafers are still in process to complete contact and metal processing. Note the gate oxide was often damaged by probes when silicide layer was used in the gate oxide integrity experiment (Voltage ramping at a constant current). The completion of metal layer will allow an investigation of the gate oxide integrity. The gate oxide defect density can be evaluated after the completion of both DOI lots. To date we have no data regarding this important parameter for the 100 Å gate oxide.

The gate oxide thickness of these two lots was measured to be 99 Å. The 99 Å gate oxide was grown at 780 °C in wet oxygen instead of baseline 850 °C wet oxygen growth. The evaluation of these wafers pulled at the silicide step will enable us to adjust the well dopings of the first baseline 0.35 CMOS lot. Radiation properties of the 99 Å gate oxide are being evaluated.